Muya Chang

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Objective

I have broad range of interests from circuit design to high-level software programming. During the ECE PhD program I focused on ASIC and Low-Power IC Design for parallel computing in optimization/ML problems, where I had taped out 10+ chips, gained familiarity with mix-signal and digital flow, and built the tape-out infrastructure for the entire lab. For the most recent project, I had the chance to experience the hierarchy from integrating a ARM Cortex M3 core into the chip attached with our mix-signal block via AMBA protocol in RTL, taping it out with TSMC 40nm technology, building the customized PCB board around it, developing the firmware for it, building a python-based interactive and user-friendly terminal, and finally running real-time application on the whole system. Aside from the ECE PhD program, I pursued a M.S. in Computer Science as my second major concurrently where I aimed to solidify my programming foundation and focused on operating systems, distributed computing, and high performance computing.

Education

Dec 2020 | **Ph.D** in **Electrical & Computer Engineering** — Advisor: Arijit Raychowdhury
Aug 2016 | **Georgia Institute of Technology**, Atlanta, GA, USA — GPA: 4.00/4.00
Specialization: **Very Large Scale Integration (VLSI)** — Detailed list of courses

May 2020 | **M.S** in **Computer Science**
Aug 2019 | **Georgia Institute of Technology**, Atlanta, GA, USA — GPA: 3.90/4.00
Specialization: **Computing Systems** — Detailed list of courses

May 2014 | **Exchange student** in **Electrical & Computer Engineering**
Jan 2014 | **University of Illinois at Urbana-Champaign**, Champaign, IL, USA — GPA: 3.79/4.00

Jun 2014 | **B.S** in **Electronics Engineering** — Advisor: Bo-Cheng Charles Lai
Sep 2010 | **National Chiao Tung University**, Hsinchu City, Taiwan — GPA: 3.90/4.00

Employment Record

Current | ASIC & VLSI Research Scientist, NVIDIA
May 2022 | Manager: Brucek Khailany

Current | Research Associate, University of Notre Dame
Dec 2021 | Supervisor: Ningyuan Cao

May 2022 | Postdoctoral Fellow at Integrated Circuits & Systems Research Lab (ICSRL), GaTech
Jan 2021 | Advisor: Arijit Raychowdhury
Topic: "SoC Design on Resistive-RAM (RRAM) with Integrated ARM Cortex M3"

Dec 2020 | Researcher at Integrated Circuits & Systems Research Lab (ICSRL), GaTech
Aug 2016 | Thesis: "Hardware Dynamical System for Solving Optimization Problems"

Aug 2019 | Interim Engineering Intern at Qualcomm Inc., Raleigh, NC
May 2019 | *CR&D Team*
- Develop near-memory computing by optimizing SRAM sub-array based on target DNN workloads for ML accelerators.

Jan 2018 | Vice President of Taiwan Student Association of GaTech, USA
Aug 2017 | - Held several events

Aug 2017 | Marketing Engineer at M2COMM Inc., Taiwan

Sep 2015	*Business Team* - Company website hosting
Sep 2014 Sep 2013	Intern at M2COMM Inc., Taiwan *Production Team & Hardware Team (2 terms)* - Team leader for building mass production auto test station
Aug 2012 Sep 2011	Vice President of Student Organization of NCTU Dept. EE, Taiwan - Fund raised up to $4000 for the department

Computer Skills

Digital Design	System Verilog, HSPICE, Synopsys Design Compiler
Physical Design	Cadence Virtuoso/Innovus/PVS, Siemens Calibre
Hardware Design	Xilinx FPGA&Vivado, Arduino, Raspberry Pi, EAGLE
Scripting Language	Perl, TCL
Serial Language	C++/C, Java, Python
Framework & API	PyTorch, Tensorflow, CUDA, OpenCL, OpenGL, OpenMP, POSIX
Revision Control	Git

Awards

Feb 2023	"Code-a-Chip" Travel Grant Awards, IEEE International Solid-State Circuits Conference (ISSCC)
Apr 2022	Best Paper Award, IEEE Opportunity Research Scholars Symposium (ORSS)
Apr 2021	Best Paper Award, IEEE Custom Integrated Circuits Conference (CICC)
May 2019	Taiwan Government Scholarship to Study Abroad (GSSA)
May 2019	Qualcomm Innovation Fellowship Award
May 2019	Chih Foundation Graduate Student Research Publication Award
Apr 2019	ECE Graduate TA Excellence Award (GaTech)
Jan 2014	Exchange Program Scholarship to University of Illinois at Urbana-Champaign (NCTU)
Jun 2011	Calculus Award (Top 20/1166) (NCTU)
Jan 2011	Calculus Award (Top 20/1202) (NCTU)
Sep 2010	Merit Scholarships in the department of Electronics & Engineering (NCTU)

Publications

1. **Stochastic Mixed-Signal Circuit Design for In-Sensor Privacy**
   J. Liu, B. Cheng, M. Chang, N. Cao
   IEEE ICCAD, 2022.

2. **Experimental Fault Rate Characterization and Protection in Embedded RRAM**
   C. Talley, B. Crafton, S. Spetalnick, M. Chang, A. Raychowdhury
   IEEE ORSS, 2022.

3. **An Analog Clock-free Compute Fabric base on Continuous-Time Dynamical System for Solving Combinatorial Optimization Problems**
   M. Chang, X. Yin, Z. Toroczkai, X. Hu, A. Raychowdhury
   IEEE CICC, 2022.

4. **A 40nm 60.64TOPS/W ECC-Capable Compute-in-Memory/Digital 2.25MB/768KB RRAM/SRAM System with Embedded Cortex M3 Microprocessor for Edge Recommendation Systems**
   M. Chang, S. Spetalnick, B. Crafton, W. Khwa, Y. Chih, M. Chang, A. Raychowdhury
   IEEE ISSCC, 2022. [Github]

5. **A 40nm 64kb 26.56 TOPS/W 2.37Mb/mm2 RRAM Binary/Compute-in-Memory Macro with 4.23x Improvement in Density and > 75% use of Sensing Dynamic Range**

S. Spetalnick, M. Chang, B. Crafton, W. Khwa, Y. Chih, M. Chang, Arijit Raychowdhury
IEEE ISSCC, 2022.

6. **A 40-nm 118.44-TOPS/W Voltage-Sensing Compute-in-Memory RRAM Macro With Write Verification and Multi-Bit Encoding**
J. Yoon, M. Chang, W. Khwa, Y. Chih, M. Chang, A. Raychowdhury
IEEE JSSC, 2022.

7. **A 40-nm, 64-Kb, 56.67 TOPS/W Voltage-Sensing Computing-In-Memory/Digital RRAM Macro Supporting Iterative Write With Verification and Online Read-Disturb Detection**
J. Yoon, M. Chang, W. Khwa, Y. Chih, M. Chang, A. Raychowdhury
IEEE JSSC, 2021.

8. **A 40nm 100Kb 118.44TOPS/W Ternary-weight Compute-in-Memory RRAM Macro with Voltage-sensing Read and Write Verification for reliable multi-bit RRAM operation**
J. Yoon, M. Chang, W. Khwa, Y. Chih, M. Chang, A. Raychowdhury
IEEE CICC, 2021.

9. **A 40nm 64Kb 56.67TOPS/W Read-Disturb-Tolerant Compute-in-Memory/Digital RRAM Macro with Active-Feedback-Based Read and In-Situ Write Verification**
J. Yoon, M. Chang, W. Khwa, Y. Chih, M. Chang, A. Raychowdhury
IEEE ISSCC, 2021.

10. **A 65nm Thermometer-Encoded Time-Based Compute-in-Memory Neural Network Accelerator at 0.735pJ/MAC and 0.41pJ/Update**
M. Gong, N. Cao, M. Chang, A. Raychowdhury
IEEE TCAS-II, 2020.

11. **EM and Power SCA-resilient AES-256 through>350×Current Domain Signature Attenuation & Local Lower Metal Routing**
D. Das, J. Daniel, A. Golder, N. Modak, S. Maity, B. Chatterjee, D. Seo, M. Chang, A. Varna, H. Krishnamurthy, S. Mathew, S. Ghosh, A. Raychowdhury, S. Sen
IEEE JSSC, 2020.

12. **A 65nm Image Processing SoC Supporting Multiple DNN Models and Real-Time Computation-Communication Trade-Off Via Actor-Critical Neuro-Controller**
N. Cao, B. Chatterjee, M. Gong, M. Chang, S. Sen, A. Raychowdhury
IEEE Symposium on VLSI Circuits, 2020.

13. **EM and Power SCA-Resilient AES-256 in 65nm CMOS Through >350x Current-Domain Signature Attenuation**
D. Das, J. Daniel, A. Golder, N. Modak, S. Maity, B. Chatterjee, D. Seo, M. Chang, A. Varna, H. Krishnamurthy, S. Mathew, S. Ghosh, A. Raychowdhury, S. Sen
IEEE ISSCC, 2020.

14. **Optimo: A 65nm 279gops/w 16b programmable spatial-array-processor with on-chip network for solving distributed optimizations via the alternating direction method of multipliers**
M. Chang, L. Lin, J. Romberg, and A. Raychowdhury
IEEE JSSC, 2019.

15. **A 65nm 8-3b 1.0-0.36v 9.1-1.1tops/w hybrid digital-mixed-signal computing platform for accelerating swarm robotics**
N. Cao, M. Chang, and A. Raychowdhury
IEEE JSSC, 2019.

16. **A ferrofet based in-memory processor for solving distributed and iterative optimizations via least-squares method**
I. Yoon, M. Chang, K. Ni, M. Jerry, S. Gangopadhyay, G. Smith, T. Hamam, J. Romberg, V. Narayanan, A. Khan, S. Datta, A. Raychowdhury
IEEE JXCDC, 2019.

17. **Efficient signal reconstruction via distributed least square optimization on a systolic fpga architecture**
M. Chang, S. Gangopadhyay, T. Hamam, J. Romberg, and A. Raychowdhury
IEEE ICASSP, 2019.

18. **65nm 49core processor array with hierarchical multicast on chip network for solving distributed optimizations**
M. Chang, L. Lin, J. Romberg, and A. Raychowdhury
IEEE CICC, 2019.

19. **14.1 a 65nm 1.1-to-9.1tops/w hybrid-digital-mixed signal computing platform for accelerating model-based and model-free swarm robotics**
N. Cao, M. Chang, and A. Raychowdhury
IEEE ISSCC, 2019.

20. **A fefet based processing-in-memory architecture for solving distributed least-square optimizations**
I. Yoon, M. Chang, K. Ni, M. Jerry, S. Gangopadhyay, G. Smith, T. Hamam, V. Narayanan, J. Romberg, S. Lu, S. Datta, A. Raychowdhury
76th DRC, 2018.

Projects

May 2022 – Jan 2021 | SoC Design on Resistive-RAM (RRAM) with Integrated ARM Cortex M3 | Language: System Verilog | Analog Portion: Virtuoso & ADE | Front End: Design Compiler | Back End: Innovus | Sign Off: PVS & Calibre
- TSMC 40nm ULP Process, chip size 5mm x 5mm
- Integrated Cortex M3 Core @ 200MHz, with 512KB RAM and 128KB ROM
- Attached our customized RRAM module onto the AMBA bus via AHB-Lite protocol
- Customized PCB board & Python based interactive terminal [Github]
- End-to-End MNIST Inference with static quantized (int8) network from PyTorch [Video]
- Presented in ISSCC 2022 Regular Paper Session 16.3 [Video]
- Participated in ISSCC 2022 Demo Session 16.3 [Video]
- Publications: ISSCC 2022 (*2)

Jan 2021 – Jan 2020 | Resistive-RAM (RRAM) Macro Design | Tool: Cadence Virtuoso
- TSMC 40nm ULP Process, chip size 3mm x 3mm
- Publications: ISSCC 2021, CICC 2021, JSSC 2021, JSSC 2022

Spring 2020 | Sharded Key/Value Service based on Paxos | Language: Java
- Linearizable key/value storage system that "shards" the keys over a set of replica groups
- Replica group & Shard master are both based on Paxos

Fall 2019 | VASN: Visualization and Analysis of Scholar Network | Language: Python/Javascript
- Visualize quantity/quality of the publication for each scholar/school
- Visualize the connection between scholars

Spring 2019 | Distributed Key-Value Store | Language: C/C++
- Use RPC (Remote procedure call)
- Focus on scalability, availability, and resilience to temporary node failures
- Reference: Dynamo - Amazon's Highly Available Key-value Store

Spring 2019 | LRVM (Lightweight recoverable virtual memory) | Language: C
- Offer persistence and crash recovery guarantees
- Use recoverable virtual memory

Spring 2019 | Inter-process Communication Services | Language: C
- Use IPC (Inter-Process Communication) and shared memory

- Support synchronous/asynchronous service calls
- Support QoS (Quality of Service)

Spring 2019 | Xen Credit-based schedulers | Language: C
- Support multi-processor
- Support local runqueue
- Support thread yield

Spring 2019 | Variation-Aware SWAP-based BidiRectional heuristic search algorithm (SABRE) | Language: Python
- Environment: IBM Q Melbourne (14 qubits)
- Metrics: Effective improvement in PST and compile time

Fall 2018 | Chip-Multiprocessor Memory System Emulator with OoO Pipeline & Precise Exceptions | Language: C/C++
- Multi-core & Multi-level cache emulator with DRAM based main memory

Spring 2018 | Post-Dominator (PDOM) algorithm for branch divergence in GPUs | Language: C/C++
- Implemented with mini-harp parallel processor
- Thread Block Compaction (TBC) supported

Spring 2018 | Sobel Operator based Image Edge Detection on FPGA | Language: Verilog
- Extracted pixels from an image and convolved with sobel kernel for edge detection

Fall 2017 | 512x512 Pixels Mandelbrot Set Display using OpenGL & CUDA | Language: C/C++
- Use CUDA & OpenGL API to compute and display a visual image of the *Mandelbrot Set*

Spring 2017 | 45nm 1.81GHz 6T SRAM Array Design with Bubble Razor and SSCFF @ Vdd=1V | Tool: Cadence Virtuoso
- Front-End design : Bubble Razor, SSCFF, and full-system design

Fall 2016 | High Speed and Low Power 45nm 1.9GHz 6T SRAM Array @ Vdd=1V | Tool: Cadence Virtuoso
- Front-End design : SRAM peripherals, SRAM cell, Sense Amplifier, and Full-System Design
- Back-End design : Full-System layout with clean DRC & LVS & PEX

Fall 2016 | A Low Power Noise Cancelling Wideband Direct Down-Conversion Receiver @ Vdd=1.2V | Tool: Agilent ADS
- Target : IEEE 802.11 a/g WLAN standard with 2 frequency bands of 2.4GHz and 5GHz
- LNA Architecture : Differential common gate LNA with noise-cancelling
- Mixer Architecture : Gilbert mixer

Course List

ECE Ph.D. Program at GaTech, Atlanta

Course #	Course Name	Instructor	Term	Grade
ECE 8853	Intro to Quantum Systems	Moinuddin K. Qureshi	Spring 2019	A
ECE 6500	Fourier Tech & Signal Analysis	David Citrin	Spring 2019	A
ECE 8823	GPU Architecture	Sudhakar Yalamanchili	Spring 2018	A
ECE 8813	Advanced Digital Design with Verilog	Timothy J Brothers	Spring 2018	A
ECE 6133	Physical Design Automation-VLSI	Sung Kyu Lim	Spring 2018	A
ECE 8843	Mathematical Foundations of Machine Learning	Justin Keith Romberg	Fall 2017	A
ECE 8893	Digital Systems at Nanometer Nodes	Saibal Mukhopadhyay	Spring 2017	A
ECE 6122	Advanced Programming Techniques	George F Riley	Spring 2017	A
ECE 8903	Special Problems	Arijit Raychowdhury	Fall 2016	A

Course #	Course Name	Instructor	Term	Grade
ECE 6420	Wireless IC Design	Hua Wang	Fall 2016	A
ECE 6130	Advanced VLSI Systems	Saibal Mukhopadhyay	Fall 2016	A

CS M.S Program at GaTech, Atlanta

Course #	Course Name	Instructor	Term	Grade
CS 7210	Distributed Computing	Ada Gavrilovska	Spring 2019	A
CS 7260	Internetworking Architectures and Protocols	Jun Xu	Spring 2019	A
CSE 6230	High Perf Parallel Computing	Tobin Gregory Isaac	Fall 2019	B
CSE 6242	Data & Visual Analytics	Duenhorng Chau	Fall 2019	A
CS 6220	Big Data System & Analytics	Ling Liu	Fall 2019	A
CS 6210	Advanced Operating Systems	Ada Gavrilovska	Spring 2019	A
CS 6505	Computability & Algorithms	Santosh Vempala	Fall 2018	A
CS 6290	High Perform Computer Architecture	Moinuddin K. Qureshi	Fall 2018	A

ECE Exchange Program at UIUC, Champaign

Course #	Course Name	Instructor	Term	Grade
CS 484	Parallel Programming	David A. Padua	Spring 2014	B
ECE 350	Fields and Waves II	Erhan Kudeki	Spring 2014	A
ECE 417	Multimedia Signal Processing	Mark Hasegawa-Johnson	Spring 2014	A+
ECE 483	Analog IC Design	Pavan Kumar Hanumolu	Spring 2014	A

References

Name	**Dr. Arijit Raychowdhury**
Title	Professor, Steve W. Chaddick School Chair, GaTech (Atlanta GA, USA)
Contact	arijit.raychowdhury@ece.gatech.edu
Relation	Advisor (Aug 2016 - Dec 2020)

Name	**Dr. Keith Bowman**
Title	Principal Engineer and Manager, Qualcomm (Raleigh NC, USA)
Contact	kbowman@qti.qualcomm.com
Relation	Manager (May 2019 - Aug 2019)

Name	**Dr. Justin Romberg**
Title	Schlumberger Professor, GaTech (Atlanta GA, USA)
Contact	jrom@ece.gatech.edu
Relation	Research co-advisor (Sep 2016 - Dec 2020)

Name	**Dr. Tushar Krishna**
Title	Associate Professor; ON Semiconductor Junior Professor, GaTech (Atlanta GA, USA)
Contact	tushar@ece.gatech.edu
Relation	Research committee (Nov 2019 - Dec 2020)